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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/625,588

07/24/2003

Takashi Kono

67161-061

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7590

09/02/2004

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EXAMINER

TRAN, MICHAEL THANH

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/625,588

Applicant(s)

KONO ET AL.

Examiner

Michael t Tran

Art Unit

2818



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2, 4, 5 and 7 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☒ Claim(s) 3 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 072403.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 24, 2003, claims 1-7 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed July 24, 2003 has been considered.

Claim Objections

4. Claims 3 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In claims 1 and 2, line 10, it is not understood how the sub-word line driver zones and the sense amplifier zones intersect each other. Do they intersect physically or electrically?

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claim 1 is rejected, as understood, under 35 U.S.C 102(b) as being anticipated by Tomishima et al. [U.S. Patent #6,147,925].

With respect to claim 1, Tomishima et al. disclose a semiconductor memory device, comprising: a plurality of memory cells [MSB10 and MSB11 of figure 17] arranged in a matrix of rows and columns; a plurality of word lines [WLs of figure 4] arranged corresponding to a plurality of column rows in said plurality of memory cells [columns and rows are interchangeable]; a plurality of bit line pairs [BLs of figure 4] arranged corresponding to a plurality of columns in said plurality of memory cells [columns and rows are interchangeable]; a plurality of sense amplifier zones [Sak and MAP of figure 21] detecting and amplifying data read from said plurality of memory cells; and a plurality of sub-word line driver zones [SW0-SW1 of figure 17] intersecting each of said plurality of sense amplifier zones; wherein each of said plurality of sense amplifier zones includes a plurality of sense amplifiers [see figures 17 and 21] provided

corresponding to said plurality of bit line pairs and detecting and amplifying a potential difference between the corresponding bit line pair, a sense amplifier driving line [Si of figure 21] provided in common to said plurality of sense amplifiers, and a plurality of first data line pairs [MI/O and ZMI/O of figure 21] provided corresponding to said plurality of bit line pairs and each selectively connected to a corresponding bit line; the semiconductor memory device further comprises a plurality of sub-amplifiers [SAK of figure 21] provided corresponding to each of said plurality of first data line pairs; each of said plurality of sub-amplifiers includes first, second, and third [Q5 or Q6 or any transistors within the sense amplifier – see column 9, lines 15-25] transistors; said first transistor has a control terminal connected to one line of said first data line pair, a first conductive terminal connected to another line of said first data line pair, and a second transistor has a control terminal connected to another line of said first data line pair, a first conductive terminal connected to one line of said first data line pair, and a second conductive terminal connected to the first conductive terminal of said third transistor; and said third transistor has a control terminal receiving an activation timing control signal [Phi.SOP. of figure 30] for said sub-amplifier, and a second conductive terminal connected to said sense amplifier driving line [these are similar to prior art structure of figure 30].

Allowable Subject Matter

7. Claims 2, 4, 5, and 7 are allowable over the prior art of record.
8. The following is an Examiner's statement of reasons for the indication of

allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- ❖ Each of said plurality of sub-word line driver zones includes a plurality of second data line pairs provided corresponding to said plurality of first data line pairs and receiving data amplified via said sub-amplifier of corresponding said first data line pair in reading.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran
Art Unit 2818
September 1, 2004